REMARKS

This amendment is submitted in conjunction with a Request for Continued Examination under 37 CFR § 1.114. In the Office Action dated October 26, 2004, the Examiner rejected Claims 1, 3-10 and 12-19. This action was made Final. Applicant has amended Claims 1, 4-6, 10 and 13-15. Claims 1, 3-10 and 12-19 are pending after entry of this amendment.

I. Response to Examiner's Remarks

In the Examiner REMARKS section, Examiner further states "testing of memory address portion as opposed to testing of entire memory address space, are not persuasive such is not in the claims at bar, which recite ' wherein the address spaces comprises x addresses and y addresses of the device,' implying that the entire memory is tested." Office Action, p.1, sec. 1.4. Applicants have amended claims 1 and 10 and respectfully point out that the pertinent step in both claims 1 and 10 recites, "determining a portion of an address space to test for determining an occurrence of a fail type, wherein ..." The address space does comprise x addresses and y addresses, but only a portion of an address space is determined for a fail type as recited in claim 1. The portion of the address space that could be tested ranges throughout the memory space. This amendment has not changed the scope of the subject matter of claims 1 and 10 related to patentability, and Applicants submit that claims 1 and 10 are in condition for allowance.

II. Rejection of Claims under 35 USC § 112, Second Paragraph

Examiner rejected claims 5-6 and 14-15 under 35 USC § 112, second paragraph for failing to particularly point out and distinctly define the subject matter which the Applicants regard as the invention. Applicants have amended claims 5-6 and 14-15 to provide the proper antecedent basis for all claim terms. The amending of these claims has not changed the scope of the subject matter related to patentability.

III. Rejection of Claims 1, 3-9 under 35 USC § 103(a)

Claims 1, 3-9 are rejected under 35 USC § 103(a) as being unpatentable over Kalter et al. (US Patent No. 5,961, 653) in view of Schanstra et al. "Semiconductor Manufacturing Process Monitoring Using Built-In Self-Test for Embedded Memories" in further view of Hosokawa et al. (US Patent No. 6,651,206).

Claim 1 recites a method for determining a fail string for a device with the following steps. The method determines a portion of an address space to test for determining an occurrence for a fail type. The method executes a test pattern at least two times for each address. The fail string is determined including the pass/fail result for the test pattern, where different subsets of the fail string correspond to different fail types. The occurrence of the fail type is determined according to the pass/fail results of a subset of the fail string.

Kalter discloses a processor-based BIST for testing DRAM in an integrated circuit. In particular, Kalter discloses a system and method that tests each subset of the memory array in the same sequence until the complete memory is tested. *See* col. 8, ll. 10-13.

Schanstra also discloses a BIST for testing DRAM. When the memory is tested, a bitmap is formed as a topological representation of the pass/fail results. The BIST is capable of capturing column faults and single cell faults. *See* Sect. 6, page 881.

Hosokawa discloses a method for performing compaction storage. In particular, Hosokawa provides compaction storage for test sequences. *See* Col. 21, ll. 56-59. Hosokawa discloses a method for generating test patterns and sequences where the sequence is generated for a given circuit. Hosokawa then sequentially compaction stores the test sequences generated for respective faults in buffers. This reference in combination with the previously cited references does not suggest or teach all of the elements recited in claim 1. Specifically there is no teaching of a fail string or even the suggestion of a subset of a fail string that corresponds with a fail type, both at the very least elements of claim 1. Thus, the elements in claim 1 remain nonobvious.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second,

there must be a reasonable expectation of success. Finally, the reference or references must teach or suggest all of the claim limitations. MPEP § 706.02(j). Contrary to the Examiner's assertion, the combination of Kalter, Schanstra and Hosokawa do not teach all of the claim limitations.

At the very least, all of the rejected claims include the step of determining a portion of an address space. Further, the rejected claims include a step of determining a fail string wherein different subsets of the fail string correspond to different fail types. Further, the failure of the fail type is determined according to the pass/fail result of a subset of the fail string. The references of Kalter, Schanstra and Hosokawa do not teach or disclose the pass/fail result in the subsets of fail strings.

In fact, Schanstra teaches away from the use of subsets to determine a fail type. In particular, Schanstra demonstrates a method of having the address "walk in the fast-row direction to determine a column fault. *See* Figure 8. He further states, "This way, cells are tested column by column." *See* Section 3.3.4, p. 877. Schanstra's method teaches a complete testing of all cells in the column.

Hosokawa's method achieves the compaction storage of shorter test sequences for various FAULTs (Fault A, Fault B, etc.) for testing integrated circuits. *See* col. 23, ll. 13-59. Further, Hosokawa determines a test sequence that will be stored once the length of the test sequence matches a buffer length that was previously set. Hosokawa neither suggests nor discloses that a portion of an address space may be tested for a failure type, nor does Hosokawa suggest that the pass/fail results of the subset of the fail string can determine a fail type. Moreover, Hosokawa does not teach or suggest a method for determining a fail string for a device wherein different subsets of the fail string correspond to different fail types. Hosokawa simply selects flip-flops to test in the integrated circuit and compaction stores the test sequence.

Applicant is unsure whether the Examiner cited **IBM Tech 7** in reference to just claim 8 or to claims 1, 3-9. Regardless, Applicants traverse the rejection of claims 1, 3-9 under 35 USC § 103(a) over Kalter in view of Schanstra, Hosokawa and in further view of the **IBM Tech 7** reference as being obvious.

IBM Tech 7 is similar in principle to Hosokawa in that the reference stands for generating a test sequence in order to avoid the distribution of undetected errors. **IBM,** First page, sixth sentence. In the IBM system, the signatures of the results of

the tested cards will be compared to the signatures of good cards. **IBM**, First page, fifth sentence. This technique does not identify the fail type, only that the card failed.

Although **IBM Tech 7** discloses a method for reducing the test circuitry in the BIST, the reference does not disclose a method for detemining a fail type as recited in claim 1. Further, the reference does not teach or suggest that the fail type could be determined from the occurrence of the pass/fail results of a subset of a fail string much less the results of a fail string. Although the combination of the previously mentioned references may utilize a particular test pattern, there is no suggestion or teaching from a combination of the references that a fail type may be determined from the pass/fail result of a subset of a fail string as recited by claim 1, only that the test passes or fails. Thus, at the very least, the claim element that recites the occurrence of the fail type be determined according to the pass/fail result of a subset of the fail string is entirely missing from the combination of the cited references. For this reason, the rejection to claim 1 should be withdrawn.

Claims 3-9 are rejected under 35 USC § 103(a) as being unpatentable over Kalter et al. (US Patent No. 5,961, 653) in view of Schanstra et al. " Semiconductor Manufacturing Process Monitoring Using Built-In Self-Test for Embedded Memories" in further view of Hosokawa et al. (US Patent No. 6,651,206). As stated above, claim 1 contains patentable limitations that are not taught or suggested by Kalter alone or in combination with Schanstra and Hosokawa and **IBM Tech 7**. Therefore, claims 3-9, which depend from patentable claim 1, are patentable for at least the same reasons. The Applicants, therefore, respectfully request the examiner to withdraw his rejection to claims 3-9.

IV. Rejection of Claims 10, 12-17 under 35 U.S.C. §103(a)

Claims 10, 12-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kalter (US Patent 5,961,653) in view of Schanstra et al., "Semiconductor Manufacturing Process Monitoring Using Built-In Self-Test For Embedded Memories" in further view of Hosokawa (US Patent 6,651,206).

Claim 10 recites a method for determining a portion of an address to test and execute a test pattern at least two times, once at a first potential and once at a second potential. The method further recites that a fail string will be determined and a pseudo compressed bit map will be generated. Finally, a failure of the device will be diagnosed according to the pseudo compressed bitmap.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met and were stated earlier. Again, the third criterion, that the reference or references must teach or suggest all of the claim limitations, is not satisfied. MPEP§706.02(j). Contrary to the Examiner's assertion, the combination of Kalter, Schanstra and Hosokawa do not teach all of the claim limitations of claim 10 either.

Claim 10 and claims 12-17, which are dependent upon claim 10, include the steps of determining a fail string for the device including a pass/fail result for the test pattern wherein a different subset of the fail string corresponds to a different fail type; generating a pseudo compressed bitmap by combining one or more subsets of the fail string; and diagnosing a failure of the device according to the pseudo compressed bitmap. The references of Kalter, Schanstra and Hosokawa do not teach or disclose, at the very least, either the pass/fail result in the subsets of fail strings, the generating of a pseudo compressed bitmap or the diagnosing a failure of the device according to the pseudo compressed bitmap.

As stated earlier, Kalter discloses a system and method that tests each subset of the memory array in the same sequence until the complete memory is tested. This is much different than determining a portion of an address space for determining an occurrence of a fail type. Kalter tests the whole memory rather than determining a portion of the memory to be tested.

Schanstra's BIST for testing DRAM forms a bitmap as a topological representation of the pass/fail results. The bitmap formed is for the entire memory array and does not take the form of a pseudo compressed bitmap.

Hosokawa's test sequences match a buffer length that was previously set, and Hosokawa neither suggests nor discloses a method for using the pass/fail results of the subset of the fail string to determine a failure type. The Hosokawa test sequence that is stored is not the same as a pseudo bitmap generated from the pass/fail result for the test pattern by combining one or more subsets of the fail string. The test sequence is simply different than the test results. Even in combination, the above references would not suggest or teach the pseudo compressed bitmap and the diagnosing of the failure according to the pseudo compressed bitmap. Thus, at the very least, the claim elements requiring the generating of the pseudo compressed bitmap and the diagnosing of the failure according to the pseudo compressed bitmap are entirely missing from the cited references. For this reason, the rejection to claim 10 should be withdrawn.

Claims 12-19 are rejected under 35 USC § 103(a) as being unpatentable over Kalter et al. (US Patent No. 5,961, 653) in view of Schanstra et al. " Semiconductor Manufacturing Process Monitoring Using Built-In Self-Test for Embedded Memories" in further view of Hosokawa et al. (US Patent No. 6,651,206). As stated above, claim 10 contains patentable limitations not suggested or taught by Kalter, alone or in combination with Schanstra and Hosokawa. Therefore, claims 12-19, which depend from patentable claim 10, are patentable for at least the same reasons. The Applicants, therefore, respectfully request the examiner to withdraw his rejection of claims 12-19.

V. Double Patenting (non-statutory)

The Applicant's request that the double patenting rejection be held in abeyance until a determination of allowable subject matter has been made.

VI. Rejection of Claims 1, 3-10 and 12-19 under 35 U.S.C. § 102

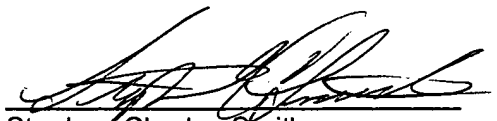
Claims 1, 3-10, 12-19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Vollraith et al. (U.S. Patent 6,564,346 ("the '346 patent)). Vollraith is a common inventor, however, the rejection under 35 U.S.C. § 102(e) is improper because not all of the elements of independent claims 1 and 10 are anticipated by Vollraith.

Claim 1, in particular, recites a step of determining a portion of an address space to test for determining an occurrence of a fail type. Claim 10 also recites a step of determining a portion of an address space to test for determining an occurrence of a fail type. Vollraith et al. in the '346 patent do not disclose the determining of a portion of an address space. Therefore, claim 1 and 10 are not anticipated by the '346 patent.

Claims 3-9 and 12-19 are dependent claims depending, directly or indirectly, upon claims1 and 10, respectively. As such, these dependent claims include the limitations of claims 1 and/or 10 and are not anticipated by the '346 patent. Applicants respectfully request the Examiner to withdraw the rejection of claims 1, 3-10 and 12-19.

In view of the response above, Applicants respectfully submit that all of the pending claims are in condition for allowance, as well as the application, and seek an early allowance thereof.

Respectfully submitted,



Stephen Charles Smith
Registration No. 53,617
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200